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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/717,235
Filing Date: November 18, 2003
Appellant(s): KUBOTA ET AL.

Carlton H. Hoel
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 5/4/2007 appealing from the Office action mailed 12/11/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,545,655	Fujikawa	4-2003
4,908,710	Wakai et al.	3-1990

Admitted Prior Art - Fig. 5, 7-10 and Background of the Invention section of specification of this application

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 recites the limitation "the second direction" in line 21. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art, hereinafter APA, in view of Fujikawa (US 6,545,655 B1).

As for claim 1, APA teaches an integrated circuit for scan driving (fig. 9 and 10) being used in sequentially selecting and driving scanning lines (by using flip-flops SREG1-SREG176) in a display (display panel 102; fig. 5 and 7), which has said plural scanning lines and plural signal lines arranged crossing each other in a matrix configuration (page 2 paragraph 1), and which has a pixel arranged at each cross point (page 2 paragraph 1); in this integrated circuit for scan driving, comprising:

a chip (scan driver LSI 108), having plural output pads arranged as a column in a first direction (see output pads/terminals OUT1-OUT176 arranged vertically as shown in fig. 8, 9 and 10; page 4 paragraph 2), plural drive circuits (DR1-DR176) for driving said scanning lines to the active state through said output pads, respectively (each DR drives a corresponding OUT as shown), and plural selection circuits (SREG1-SREG176) for individually selecting said driver circuits in a line-sequential scanning cycle (each SREG does select a corresponding driver circuit DR as shown). For details see page 4 paragraph 3 through page 6 paragraph 2.

However, the correspondence between the flip-flops SREG1-SREG176 and the drivers DR1-DR176 is not in order but crisscrossed instead. Consequently, APA does not teach the plural selection circuits SREG1-SREG176 in an order corresponding to the order of said scanning lines;

the odd-numbered output pads, driver circuits and selection circuits corresponding to odd-numbered scanning lines are all arranged in a first region,

the even-numbered output pads, driver circuits and selection circuits corresponding to the even-numbered scanning lines being all arranged in a second region adjacent to said first region in said first direction;

said first region, in an order corresponding to the order of said odd-numbered scanning lines, said odd-numbered output pads, driver circuits and selection circuits being arranged as columns in said first direction, respectively, and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines are arranged in the same row in the second direction nearly orthogonal

to said first direction; and,

in said second region, in an order corresponding to the order of said even-numbered scanning lines, said even-numbered output pads, driver circuits and selection circuits are arranged as columns in said first direction, and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines being arranged in the same row in said second direction.

Fujikawa also teaches an integrated circuit for scan driving (vertical driver IC 33; fig. 6). Specifically, Fujikawa teaches two vertical drivers 25 and 26 formed adjacent to each other vertically in the vertical driver IC 33 (column 12 lines 41-53). Moreover, Fujikawa teaches that vertical driver 25 is for selecting pixels along odd-numbered rows and vertical driver 26 is for selecting pixels along even-numbered rows (column 13 lines 1-5). Further, the connections from the drivers 25 and 26 to the LCD panel 8A are clearly shown as crisscrossed in order to connect from odd outputs to odd rows and even outputs to even rows.

One of ordinary skill in the art would recognize by utilizing Fujikawa's teaching APA's correspondence between the selection circuits SREG1-SREG176 and drivers DR1-DR176 can be made in order and the odd-number circuits and even-numbered circuits can be separated into two regions. It is also clear that Fujikawa's way of combining two drivers into one IC saves chip space as the crisscrossing is now formed outside the IC (see fig. 6). Therefore, it would have been obvious to modify APA's scan driving IC in view of Fujikawa's teaching because of the space saving advantage.

As for claim 5, the direction in which the two drivers 25 and 26 are aligned is in the longitudinal direction of the scan driver IC 33. As shown in fig. 10 of APA, the output pads are clearly formed along one edge.

As for claim 6, it is inherent that there are input pads or terminals in order to receive inputs such as CPV and STV as shown in fig. 8 and 10 of APA.

As for claim 7, as shown in fig. 7, the scan driving IC 108 of APA is mounted on a TCP (page 2 paragraph 3).

5. Claims 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA and Fujikawa as applied to claim 1 above, and further in view of Wakai et al. (US 4,908,710), hereinafter Wakai.

Claim 8's first shift register, first drive section, second shift register, second drive section correspond to claim 1's odd-numbered selection circuits, odd-numbered driver circuits, even-numbered selection circuits, even-numbered driver circuits, respectively, and is rejected accordingly by rejection of claim 1. However, claim 8's limitation on "a second shift data shifted in phase by half a period of a second clock signal with respect to said first shift data corresponding to the second clock signal with its phase deviated by 180 from said first clock signal" is not recited in claim 1.

Both APA and Fujikawa teach using one vertical clock for driving the shift registers (CPV in the case of APA and VCK in the case of Fujikawa). Thus, APA and Fujikawa do not teach the above use of first and second clock signals. Wakai teaches using two clock signals (Φyo and Φye) to drive respective odd and even scanning driving circuits (fig. 4-5; column 6 lines 17-46). Further, Wakai teaches that the two

clock signals have inverse phase relation to each other (fig. 9; column 9 lines 30-32). One of ordinary skill in the art would recognize that Wakai's clock driving is a functionally equivalent alternative to modified APA's clock driving.

It would have been obvious to utilize Wakai's two clock signals driving in modified APA's scan driver IC, as both methods are functionally equivalent and would be selected based on design preference.

As for claims 9 and 12, Fujikawa's scan drivers 25 and 26 both have their register circuits and driver circuits aligned in the longitudinal axis of the IC.

As for claim 10, APA further teaches using decoders DEC1-DEC176 (fig. 9-10, part of driver circuits DR1-DR176) for controlling direction and initial stage as claimed.

As for claim 13, APA as modified by Fujikawa and Wakai has odd-numbered scan signals sequentially coming from a top driver and even-numbered scan signals sequentially coming from a bottom driver.

(10) Response to Argument

As for claim 1, Appellant argues that as the second direction is already defined by orthogonality to the first direction, thus the use of definite article "the" with "second direction" is permissible. The Examiner disagrees since the orthogonality is actually defined after the citation of the term "second direction."

As for claims 1 and 5-7, Appellant argues that Fujikawa does not show the internal arrangement of the items within v-drivers 25, 26 which relate to the claim 1 requirements. The Examiner disagrees because Fujikawa does not need to show internal arrangements regarding the output pads, drive circuits and selection circuits

because these elements are taught in the APA. Moreover, as analyzed in the rejection of claim 1, since the two vertical drivers 25 and 26 are distinctly separate and drive odd-numbered rows and even-numbered rows respectively, one of ordinary skill in the art would recognize that, by incorporating the teaching of Fujikawa, the selection circuits SREG1-SREG176 and the drivers DR1-DR176 can be made to correspond with each others in order and thus can be separated into two regions (top and bottom). This is advantageous as any crisscrossing can now be removed from within the integrated circuit, resulting in saving of chip space.

As for claims 8-10 and 12-13, Appellant argues that Wakai has shift registers 401 and 402 with clocks ϕyo and ϕye on opposite sides of the LCD panel; thus Wakai would not suggest anything about two shift registers and drivers on the same side. However, the teaching of the shift registers and drivers on the same side is already taught by the APA as modified by Fujikawa. The Examiner is only relying on the Wakai reference to teach the use of two separate clock signals ϕyo and ϕye to drive respective odd and even scanning driving circuits. Further the two clock signals have inverse phase relation to each other resulting in alternate output. Thus, the incorporation of Wakai's teaching of two separate clocks represents a functionally equivalent alternative.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Tom V. Sheng

Conferees:

Richard Hjerpe and Amr Awad

/R. H./

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